DESIGN OF A BACKGROUND MISMATCH CALIBRATION SCHEME
FOR A 10-BIT 12 GS/s 16-CHANNEL TIME-INTERLEAVED ADC IN 28 nm FD-SOI PROCESS

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Motivation
Time-interleaving is a widely used technique in high-speed ADC design. An important side effect of time-interleaving is inter-channel mismatch, which affects the output quality regardless of the quality of sub-ADCs. This work presents an implementation of a mismatch calibration scheme applied on a 10-bit 12 GS/s 16-channel time-interleaved SAR ADC. The proposed scheme is developed using and expanding the existing architectures. It consists of a digital calibration processor and a programmable delay line.

Method
Offset mismatch calibration
Mean of the output directly contains offset information. Choosing one channel as reference, mean difference gives offset mismatch, which can be subtracted from channel outputs.

Gain mismatch calibration
Absolute mean of the output indirectly contains gain information. Choosing one channel as reference, gain can be corrected iteratively until absolute means are equalized [1].

Timing mismatch calibration
Calibrating timing mismatch without interrupting the operation (background) and without explicit knowledge of the input (blind) has been demonstrated for 2 and 4 channels [2,3]. This work generalizes the architecture to N-channel TI-ADCs. The architecture depends on the cross-correlation of channel outputs, which translates to the auto-correlation of the input with a lag of $kT_c$. Difference of cross-correlations yields a value directly proportional to the timing mismatch, provided that the input and clock signals are asynchronous. The sampling clock is tuned via a programmable delay line until the mismatch is zero.

Implementation
The designed calibration scheme is integrated into a 16-channel SAR ADC and sent to be fabricated in Samsung 28 nm FD-SOI process. The calibration processor occupies an area of 250 $\mu$m by 550 $\mu$m. The programmable delay line occupies an area of 50 $\mu$m by 100 $\mu$m.

Results
The designed calibration scheme is able to restore effective number of bits (ENOB) from as low as 5 bits to 9 bits. The frequency response of the timing mismatch calibration has notches at $1/(kT_c)$. The processor dissipates 84 mW, and the delay line draws 105 $\mu$W from a 1 V supply.

Conclusion
Digital processing capabilities of scaled technologies can be leveraged to compensate for the imperfections in the analog part. It is possible to mitigate the causes and/or effects of mismatch after fabrication using digital post-processing. Linearity mismatch detection based on averaging is straightforward, and correction is simple arithmetic in digital domain. Blind background timing mismatch detection is possible without an extra channel, as long as the input signal satisfies certain conditions. For higher number of channels, correct detection gets more difficult as mismatch information gets weaker. Correction can be done via programmable delay lines. Designing multi-phase clocked digital circuits creates timing problems. A systematic approach eases the design procedure of such circuits.

References