Extremely High Speed Digital Down Converter Design for Wireless Communication Applications

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- More than 4 GHz semi-custom design of a digital down converter for time-interleaved ADC in ST 28nm FDSOI technology.
- Maximal clock frequency study by deep pipelining and semi-custom flow optimization.
- 30% delay improvement over simplistic full-adder-based structure thanks to compression tree generation algorithm based on three-greedy method.
- Dynamic true single phase clock (TSPC) DFF development and integration demonstrating 16% additional improvements.
- Test interface proposed with full tape-out layout described for Silicon measurements.

1. High speed wireless receiver

- Wireless receiver path using time-interleaved ADCs [1] and digital down conversion (DDC).
- Elimination of resource-intensive mixers if sampling fast enough \( (f_s = 4 \cdot f_c) \) [2].

2. Digital Down Converter

- DDC implements Hogenauer’s equation for CIC sections of order \( N \) [3].

\[
H(z) = \left( \sum_{k=0}^{N-1} z^{-k} \right) \sum_{k=0}^{N-1} H_k(z^N).
\]

with \( R \) sub-channel filters \( (c_{n,k} \text{ constant coefficients}) \):

\[
H_k(z) = \sum_{n=0}^{N-1} c_{n,k} z^{-n}.
\]


3. Pipelining

- Design-independent minimal delay reached by deep pipelining, adequate pipeline length and optimal registers placement.
- Delay bound decreased by changes in technology or standard cells.

4. TSPC flip-flops

- Up to 50%, resp. 70%, better setup time plus clock-to-Q delay.

Table 1: TSPC and DP TSPC clock-to-Q+setup delay metric for high speed (in ps) compared to static DFF.

<table>
<thead>
<tr>
<th></th>
<th>ST (static)</th>
<th>TSPC</th>
<th>DP TSPC</th>
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<tbody>
<tr>
<td>edge</td>
<td>sch extr</td>
<td>sch extr</td>
<td>sch extr</td>
</tr>
<tr>
<td>fall</td>
<td>51.7 61.8</td>
<td>26.0 32.1</td>
<td>12.7 19.8</td>
</tr>
<tr>
<td></td>
<td>-50% -48%</td>
<td>-75% -68%</td>
<td></td>
</tr>
<tr>
<td>rise</td>
<td>43.0 57.9</td>
<td>17.0 22.4</td>
<td>14.1 15.9</td>
</tr>
<tr>
<td></td>
<td>-60% -61%</td>
<td>-67% -73%</td>
<td></td>
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</tbody>
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Table 2: Results for \( N = 4, R = 8 \) and \( S_0 = 8 \) on parasitic-extracted views with typical process, 0.80 V supply voltage and 125 °C.

<table>
<thead>
<tr>
<th>Design</th>
<th>Core area</th>
<th>Max. freq.</th>
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<tbody>
<tr>
<td>Reference</td>
<td>[µm]</td>
<td>[GHz]</td>
</tr>
<tr>
<td>3-greedy</td>
<td>13.864</td>
<td>2.8</td>
</tr>
<tr>
<td>3-greedy TSPC</td>
<td>14.298</td>
<td>3.7 32%</td>
</tr>
<tr>
<td>3-greedy TSPC</td>
<td>15.060</td>
<td>4.3 54%</td>
</tr>
</tbody>
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Optimization steps summary:

1. DDC structure analysis and automated generation as a compression tree.
2. Deep pipelining to reach the minimal delay bound defined by technology and standard cell library.
3. TSPC flip-flops design and integration to reduce this delay bound.

References