12-bit SAR ADC for machine type communication in 130nm CMOS

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Goals

- Design 12-bit SAR ADC design in CMOS 130 nm technology
- Use an efficient energy switching scheme to save power (< 300 µW)
- Use a novel capacitive array topology to achieve a good linearity (> 70 dB SNR)
- Application: Machine to machine communication using 4G LTE at 3.84 Ms/s

Theory/Method/Hypothesis

- Top-down design flow
  
  Design using models
  
  Implement block
  
  Higher level of hierarchy
  
  Top level functional
  
  No
  
  Redesign
  
  No
  
  Layout
  
  No
  
  Transistor level
  
  Design

- Verify functionality of each block and at the top level
- Short development time with verification in early stage

- Charge redistribution capacitive array with attenuation capacitor (C = 40fF)
- Partially thermometer encoded MSBs with dynamic element matching

- Strong arm clocked comparator for no static power consumption [1]
- Input referred voltage noise dependant on C_{PD} and size of input differential pair

Results

- CSA tool: Matlab toolbox used to evaluate mismatch and its consequences in the performance of a charge redistribution SAR ADC, with simulation time up to 10^4 faster than Cadence. [2]
- Modification of the initial code to investigate new topology models, which led to the choice of this converter topology.

Transistor level FFT shows third harmonic below -77 dB.

<table>
<thead>
<tr>
<th>Power (uW)</th>
<th>OSR = 1</th>
<th>OSR = 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator</td>
<td>46.4</td>
<td>95.9</td>
</tr>
<tr>
<td>SAR Logic</td>
<td>15.6</td>
<td>30.4</td>
</tr>
<tr>
<td>Cap array</td>
<td>65.9</td>
<td>132.6</td>
</tr>
<tr>
<td>Total</td>
<td>127.9</td>
<td>258.9</td>
</tr>
</tbody>
</table>

- Power consumption mostly from comparator and capacitive array

Conclusion/Perspectives

- Top-down design flow from modeling on Matlab and verilogA to transistor level implementation in Cadence Virtuoso, with a FOM similar to state-of-art [3].

FOM3 = SNDR + 10log_{10}(BW/P)

<table>
<thead>
<tr>
<th>Sampling frequency</th>
<th>FOM3 (dB)</th>
</tr>
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<tbody>
<tr>
<td>3.84 MSps</td>
<td>173.75</td>
</tr>
<tr>
<td>7.68 MSps</td>
<td>173.6</td>
</tr>
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</table>

What has been done:

- Draw layout of each sub block, and verify the top level functionality
- Investigate ways to reduce power consumption of the chip: headroom on comparator noise

References