Design of a 2 Mb Gain-Cell Embedded DRAM in 28 nm FD-SOI

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Introduction
To cope with the emergence of new technologies, an increasing need for memory space has been observed in the last decade. SRAM memories have been widely used as the main type of volatile memories in most system-on-chip designs, however their static power consumption makes them inefficient for low-power applications, where DRAMs are usually preferred as a low-power alternative. A special type of DRAMs called Gain-cell embedded DRAMs is studied in this work, via the design of a 2 Mb hierarchical memory in 28 nm FD-SOI technology.

The target of this work was to create the densest memory within 1 mm² while ensuring single-cycle accesses for clock frequencies of at least 100 MHz.

Theory
Gain Cell
The gain cell (GC) is the atomic block which stores 1 bit of data in the form of electrical charge on an internal capacitive node. Being a dynamic memory, leakage effects cause an alteration of the stored data over time which sets a time at which the stored value needs to be refreshed. Due to the topology of gain cells, the read operation is non-destructive, allowing dual-port operations.

Hierarchical Memories
Gain cells are first grouped into words, which are grouped into arrays and then stacked to form columns, which are finally placed side-by-side to form the hierarchical memory. Global decoders are used to address the correct array, while local ones access the desired word within an array.

Results
After having performed the architectural design with the help of the Gemtoo[1] modelling tool, the schematic-level implementation achieved successful write and read operations at the farthest address. A minimal clock period of 3 ns gave correct results in simulation, leading to an operational working frequency of 333 MHz. Programmable delay lines were used to generate internal timing-critical control signals and were set to values include a significant safety margin, which could be removed to reach higher working frequencies in the range of frequencies predicted by the Gemtooo[1] model. The operational frequency obtained in this work is valid for the full 2 Mb memory, but higher clock frequencies can be reached if only a portion of the memory is needed. Finally, the layout area has been estimated at 0.56 mm² by Gemtoo[1].

Conclusions
In this work, a 2 Mb full-custom GC-eDRAM hierarchical memory reaching a working frequency of 333 MHz was successfully designed at schematic level. An optimization of the programmable delay lines is expected to boost the operating frequency to values approaching 800 MHz, and the next step would consist in drawing the layout of all full-custom blocks composing the 2 Mb hierarchical memory. Thanks to an accurate estimation of the wiring parasitics, post-layout simulations should provide satisfactory results with respect to the targeted working frequency, and the final step would be to include BIST circuitry to consider taping this memory out.

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References